#5/A 12/6/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **NAKAYAMA, Akitaka et al.**

Group Art Unit:**1765**

Serial No.: **09/713,036**

Examiner: **AHMED, SHAMIN**

Filed: **November 16, 2000**

P.T.O. Confirmation No.: **3155**

For. **METHOD OF MANUFACTURING MULTI-LAYER PRINTED WIRING BOARD**

AMENDMENT UNDER 37 CFR §1.111

Commissioner for Patents
Washington, D.C. 20231

December 4, 2002

Sir:

In response to the Office Action dated **July 5, 2002**, extended to **December 5, 2002** by a **2** month Petition for Extension of Time, please amend the above-identified application as follows:

IN THE CLAIMS:

Please **CANCEL** claims 14-16 without prejudice or disclaimer.

Please **AMEND** the claims 1and 5-13 as follows:

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1. (Amended) A method of manufacturing a multi-layer printed wiring board comprising an internal layer circuit forming step, an outer layer circuit forming step, and a solder resist forming step,

wherein the internal layer circuit forming step and the outer layer circuit forming step comprise steps of:

providing a board coated with a patterning material;

coating the surface of the patterning material with a photosensitive film;